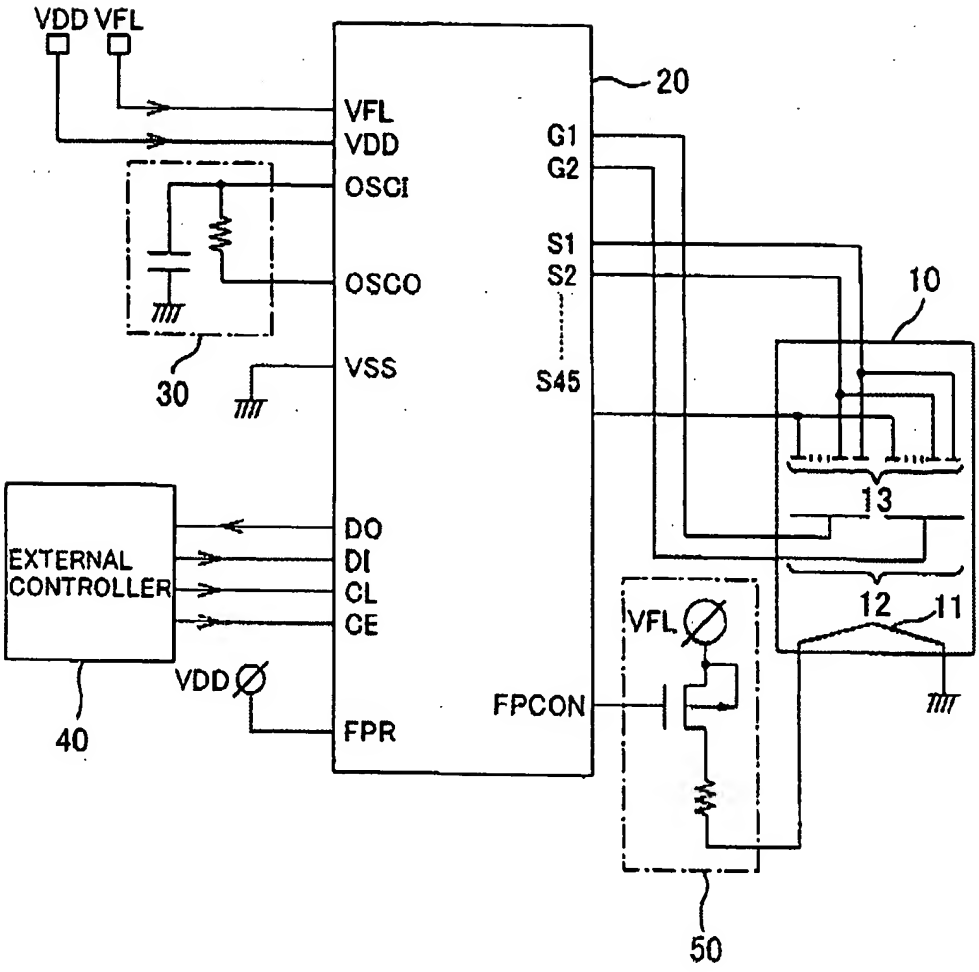

VDD VFL
VFL
VDD
OSCI
OSCO
VSS
30
20
G1
G2
S1
S2
S45
10
13
12
11
EXTERNAL CONTROLLER
DO
DI
CL
CE
VDD
FPR
40
FPCON
VFL
50

FIG.1

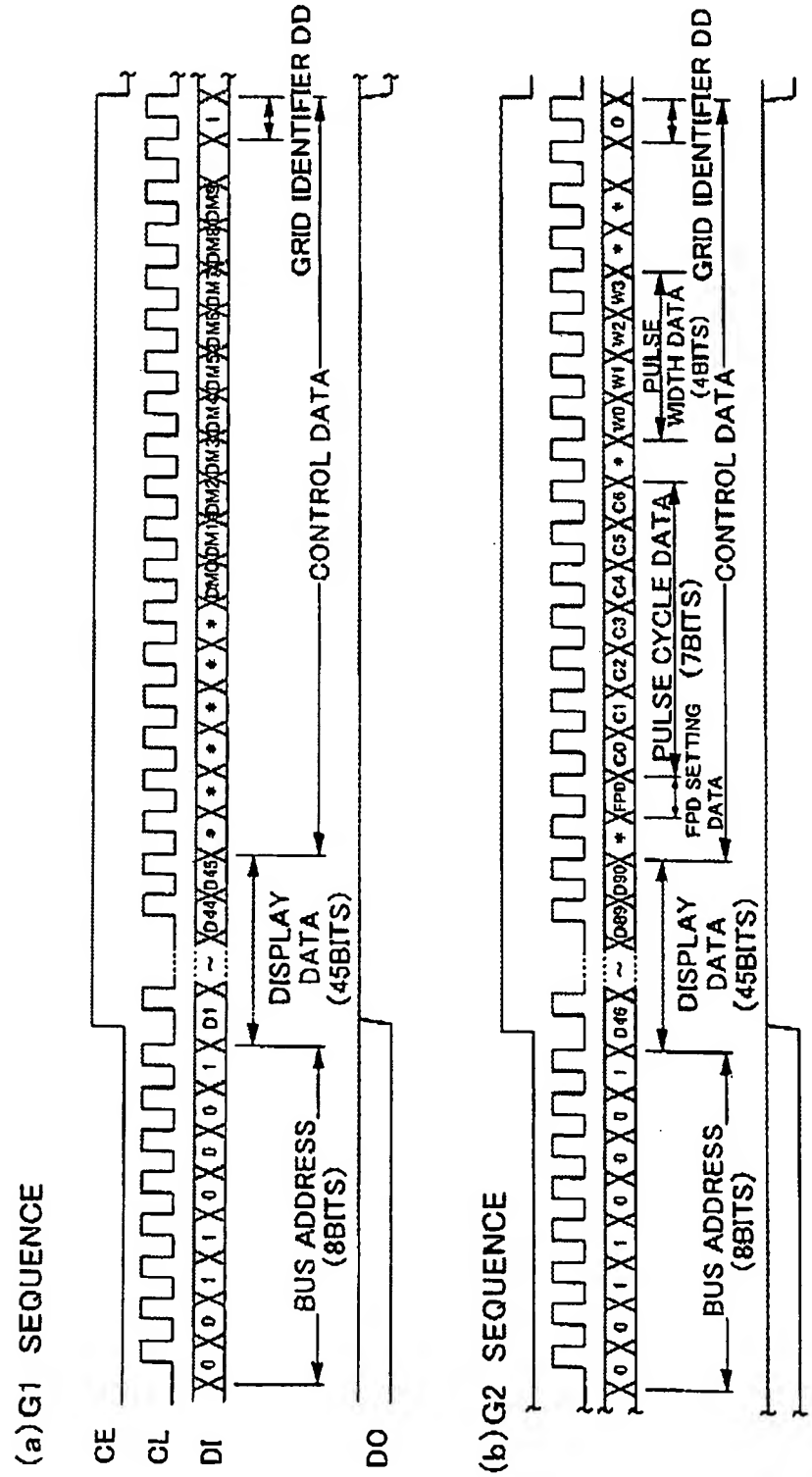

(a) G1 SEQUENCE
CE
CL
DI
DO
BUS ADDRESS (8BITS)
DISPLAY DATA (45BITS)
CONTROL DATA
GRID IDENTIFIER DD
(b) G2 SEQUENCE
BUS ADDRESS (8BITS)
DISPLAY DATA (45BITS)
FPD SETTING DATA
PULSE CYCLE DATA (7BITS)
PULSE WIDTH DATA (4BITS)
CONTROL DATA
GRID IDENTIFIER DD

FIG.2

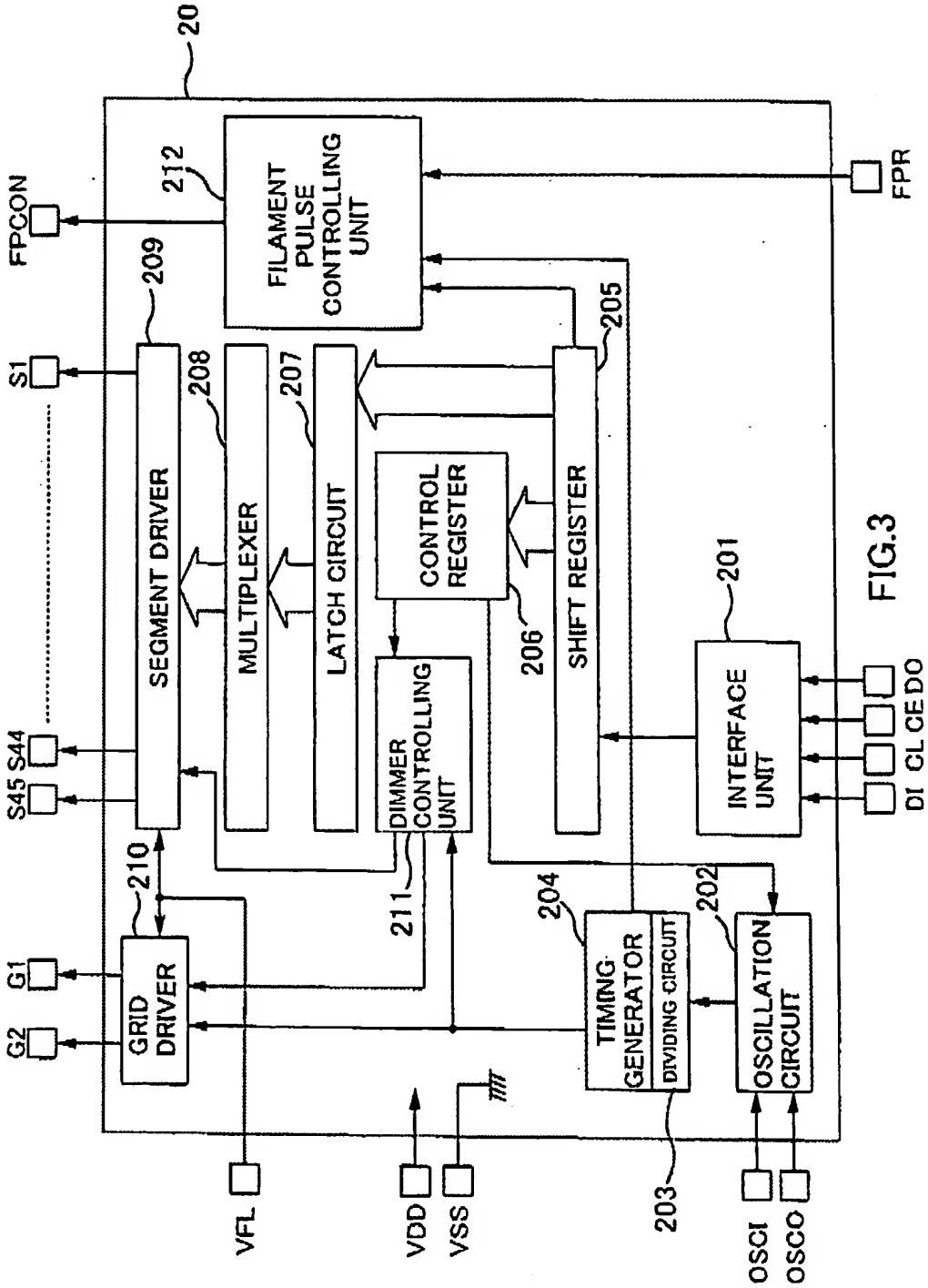

20
FILAMENT PULSE CONTROLLING UNIT
212
FPCON
FPR
209
S1
208
207
205
SEGMENT DRIVER
MULTIPLEXER
LATCH CIRCUIT
CONTROL REGISTER
SHIFT REGISTER
201
S45 S44
DIMMER CONTROLLING UNIT
206
INTERFACE UNIT
DI CL CE DO
210
211
204
202
G1
G2
GRID DRIVER
TIMING GENERATOR
DIVIDING CIRCUIT
OSCILLATION CIRCUIT
VFL
VDD
VSS
203
OSCI
OSCO

FIG.3

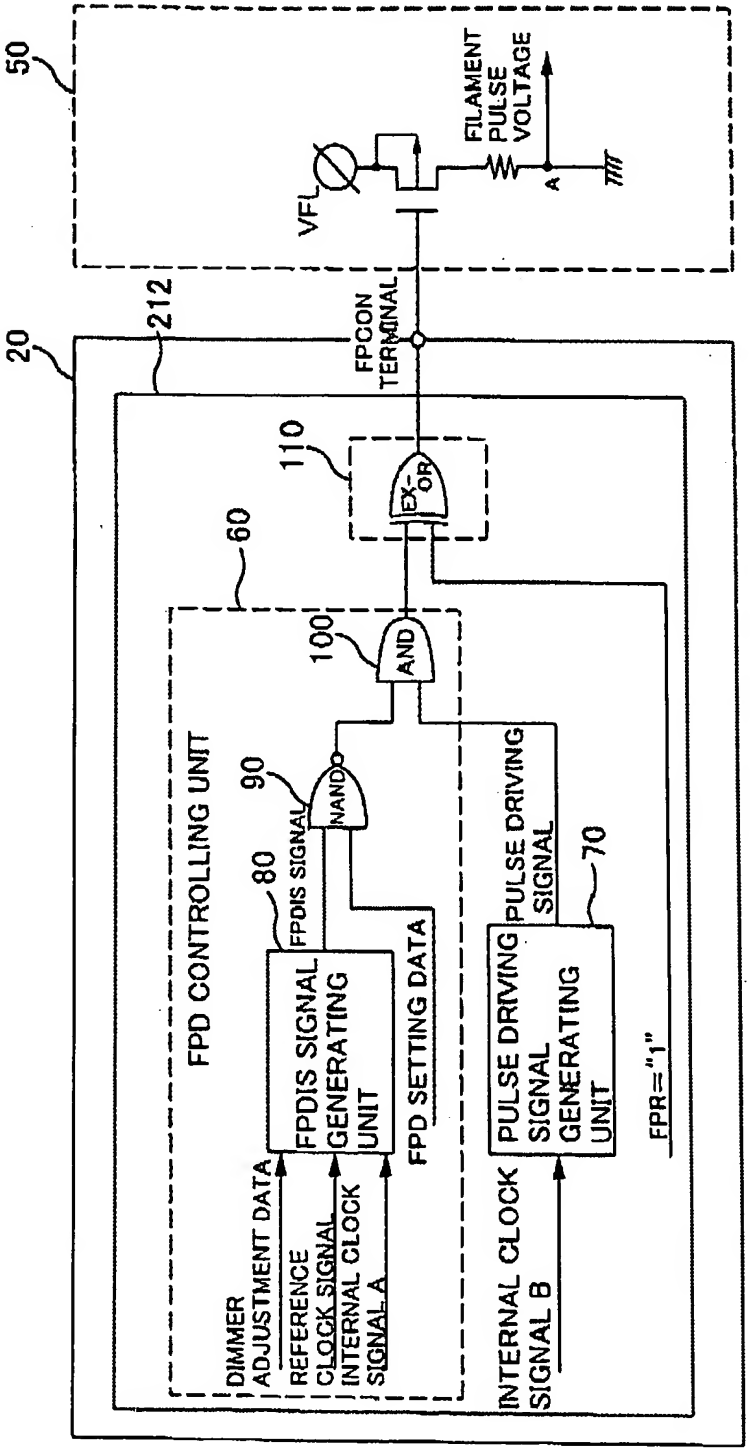

50
VFL
FILAMENT PULSE VOLTAGE
A
20
212
FPCON TERMINAL
110
EX-OR
60
100
AND
90
NAND
FPDIS SIGNAL
80
FPD CONTROLLING UNIT
FPDIS SIGNAL GENERATING UNIT
FPD SETTING DATA
PULSE DRIVING SIGNAL
70
PULSE DRIVING SIGNAL GENERATING UNIT
FPR="1"
DIMMER ADJUSTMENT DATA
REFERENCE CLOCK SIGNAL
INTERNAL CLOCK SIGNAL A
INTERNAL CLOCK SIGNAL B

FIG.4

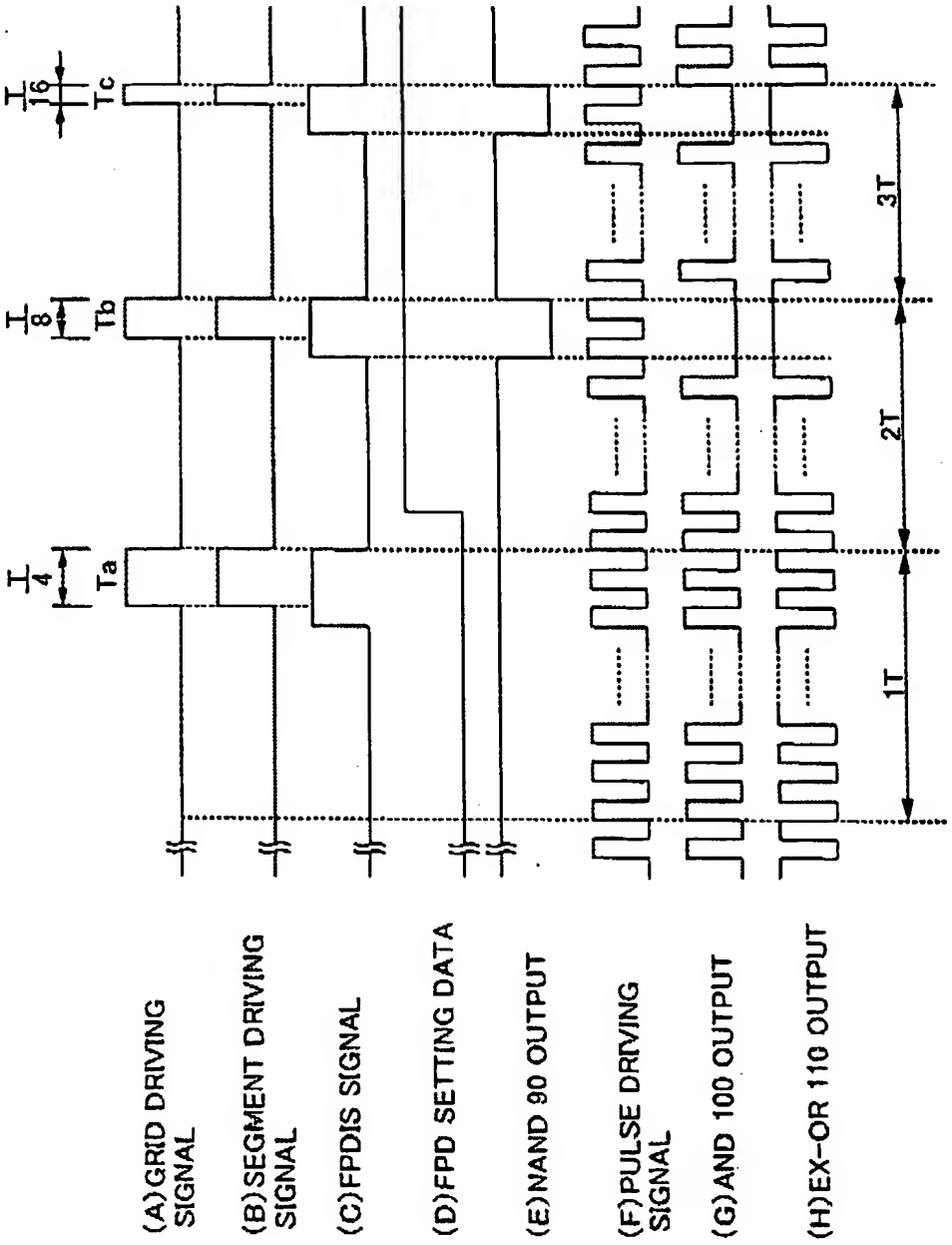

1/16
Tc
1/8
Tb
1/4
Ta
3T
2T
1T
(A) GRID DRIVING SIGNAL
(B) SEGMENT DRIVING SIGNAL
(C) FPDIS SIGNAL
(D) FPD SETTING DATA
(E) NAND 90 OUTPUT
(F) PULSE DRIVING SIGNAL
(G) AND 100 OUTPUT
(H) EX-OR 110 OUTPUT

FIG.5

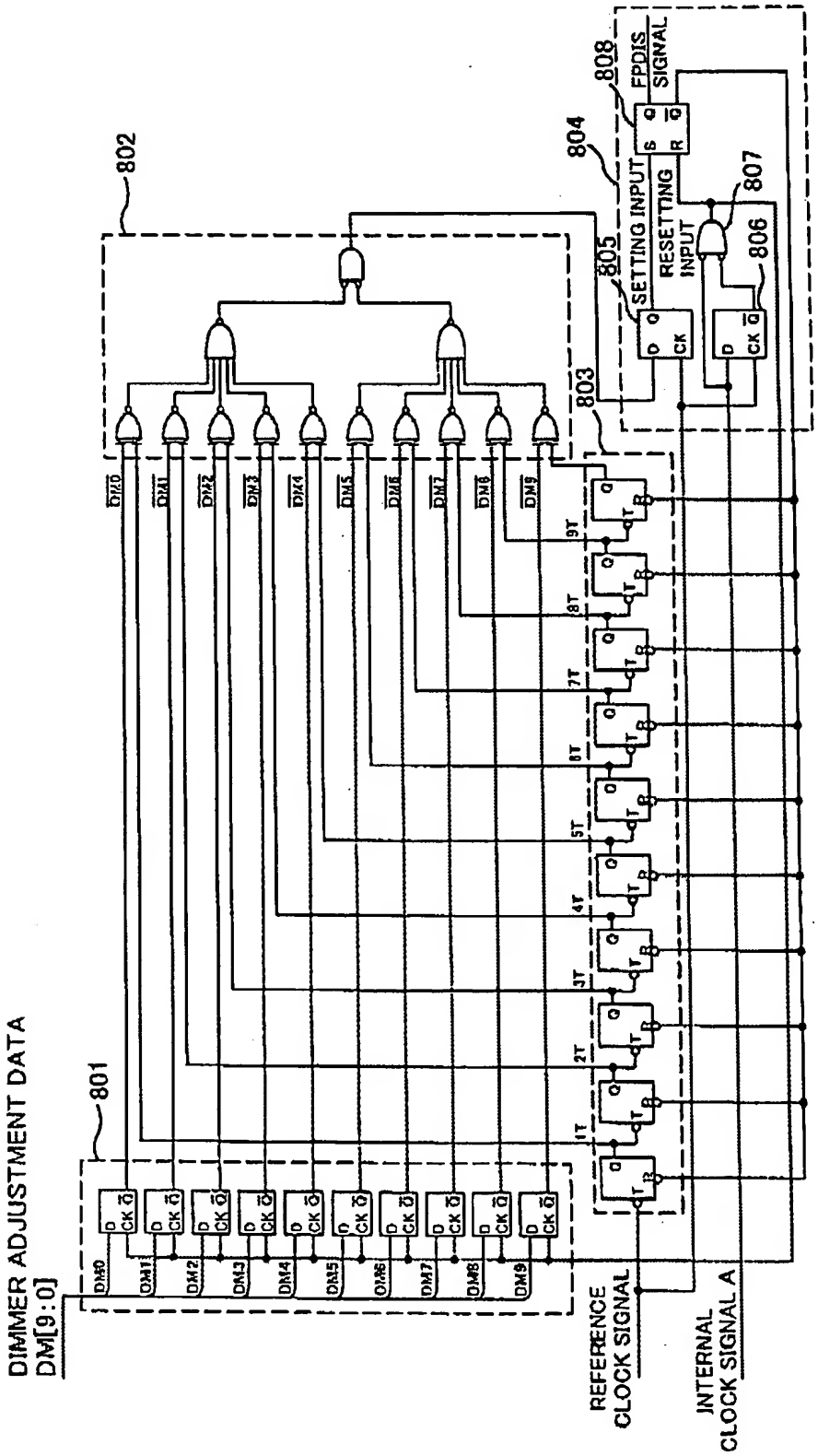

DIMMER ADJUSTMENT DATA
DM[9:0]
801
802
803
804
805
806
807
808
FPDIS SIGNAL
SETTING INPUT
RESETTING INPUT
REFERENCE CLOCK SIGNAL
INTERNAL CLOCK SIGNAL A
1T
2T
3T
4T
5T
6T
7T
8T
9T

FIG.6

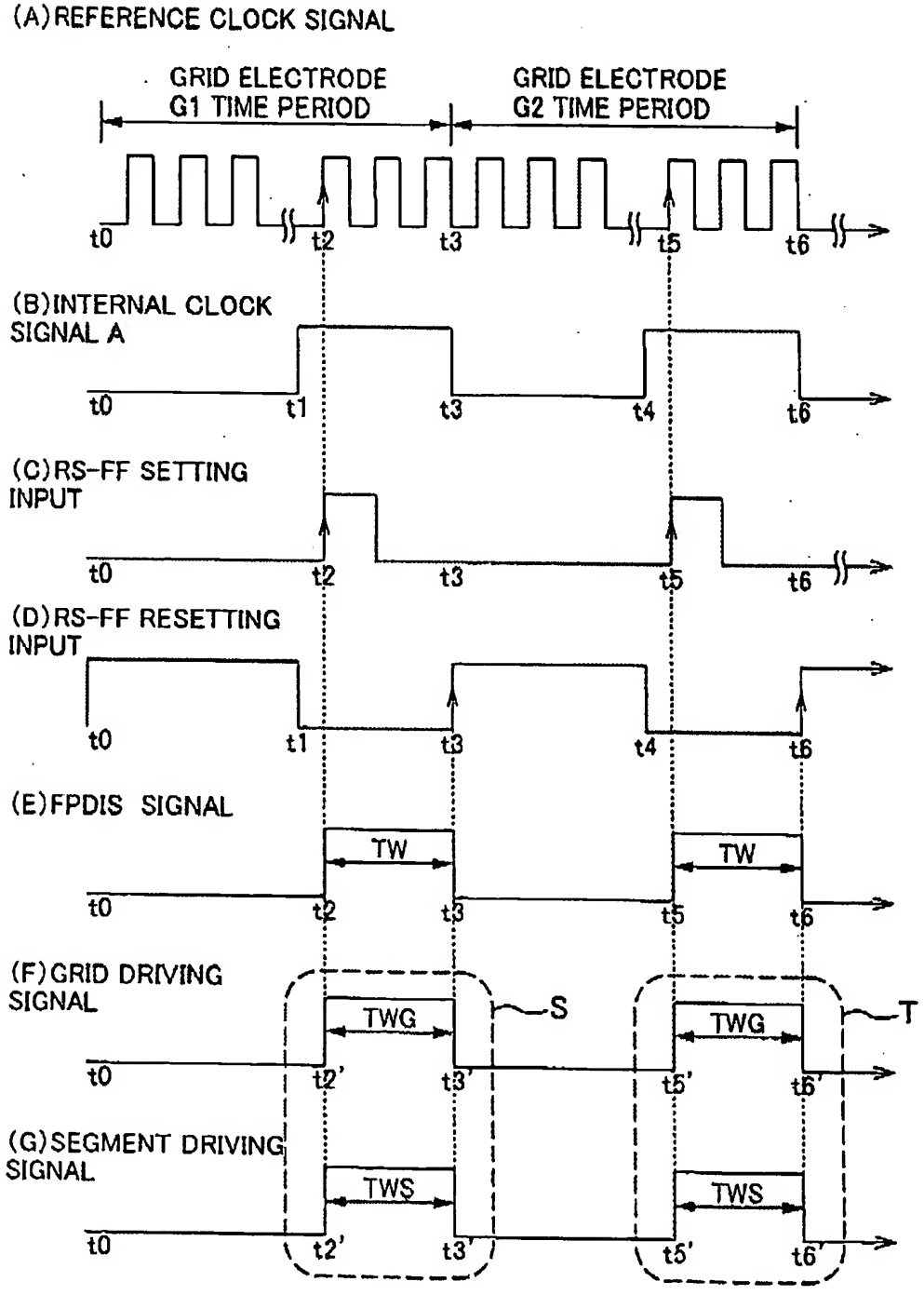

(A) REFERENCE CLOCK SIGNAL
GRID ELECTRODE G1 TIME PERIOD
GRID ELECTRODE G2 TIME PERIOD
t0
t2
t3
t5
t6
(B) INTERNAL CLOCK SIGNAL A
t0
t1
t3
t4
t6
(C) RS-FF SETTING INPUT
t0
t2
t3
t5
t6
(D) RS-FF RESETTING INPUT
t0
t1
t3
t4
t6
(E) FPDIS SIGNAL
TW
TW
t0
t2
t3
t5
t6
(F) GRID DRIVING SIGNAL
TWG
TWG
S
T
t0
t2'
t3'
t5'
t6'
(G) SEGMENT DRIVING SIGNAL
TWS
TWS
t0
t2'
t3'
t5'
t6'

FIG.7

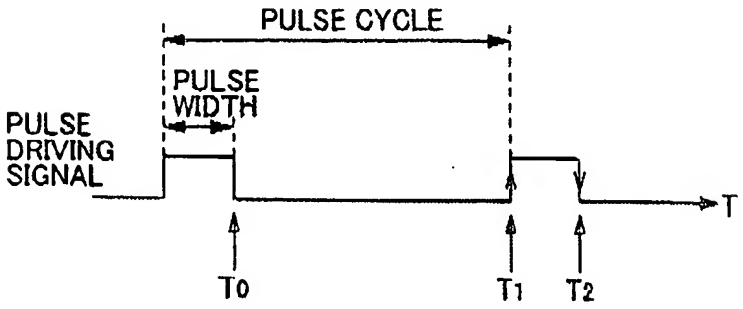


FIG.8

W3	W2	W1	W0	VALUE SET FOR Wn	FPC PULSE WIDTH
0	0	0	0	—	—
0	0	0	1	3	3/fosc
0	0	1	0	4	4/fosc
~					~
0	1	1	0	8	8/fosc
~					~
1	1	1	0	16	16/fosc
1	1	1	1	17	17/fosc

FIG.9

C6	C5	C4	C3	C2	C1	C0	VALUE SET FOR Cn	FPC PULSE CYCLE
0	0	0	0	0	0	0	—	—
0	0	0	0	0	0	1	—	—
0	0	0	0	0	1	0	4	4/fosc
0	0	0	0	0	1	1	5	5/fosc
~								~
1	0	0	0	1	1	0	72	72/fosc
~								~
1	1	1	1	1	1	0	128	128/fosc
1	1	1	1	1	1	1	129	129/fosc

FIG.10

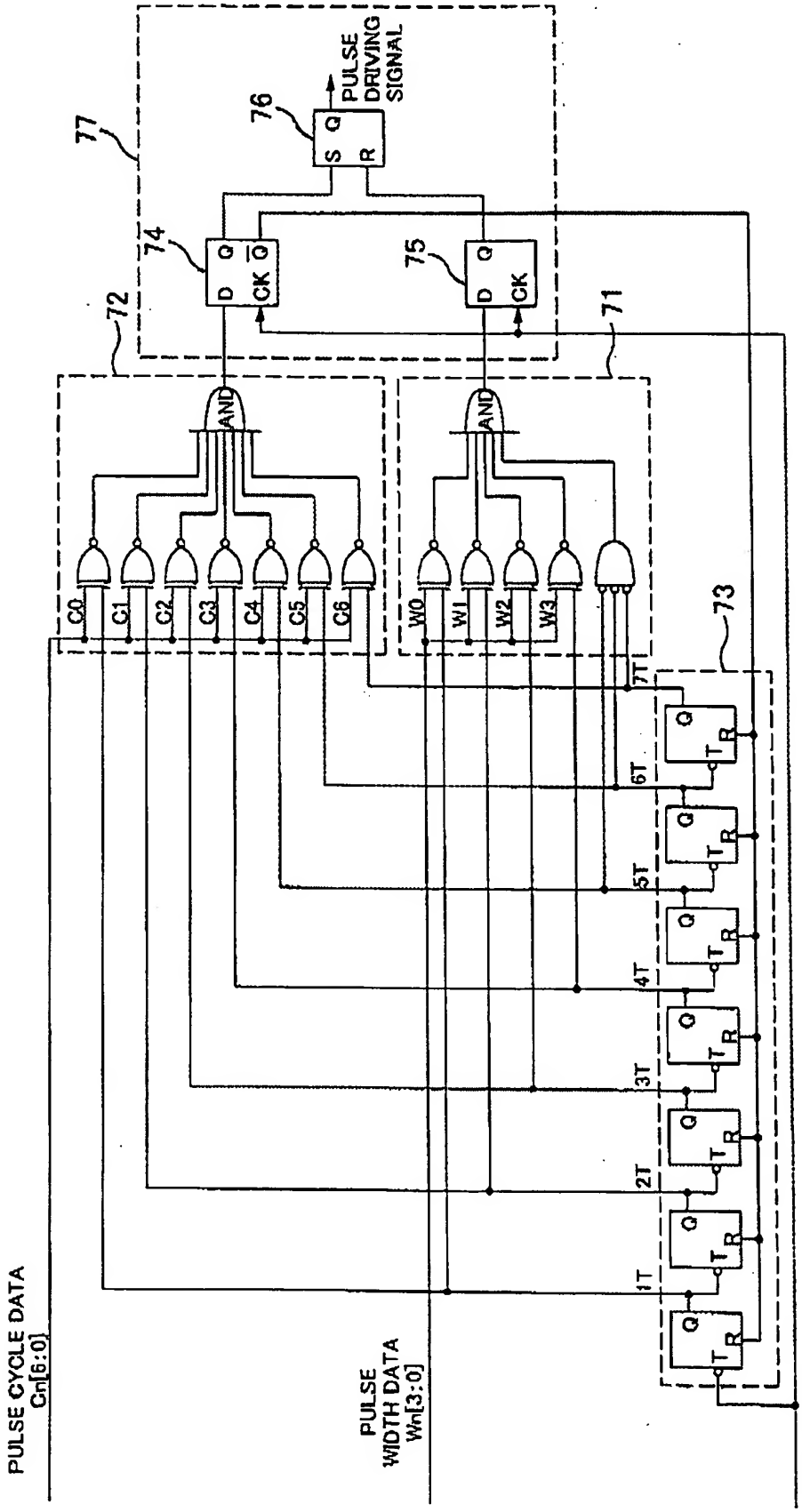
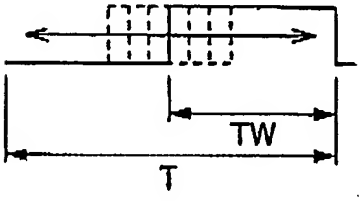

PULSE DRIVING SIGNAL
76
77
74
75
72
71
73
AND
AND
C0
C1
C2
C3
C4
C5
C6
W0
W1
W2
W3
7T
6T
5T
4T
3T
2T
1T
PULSE CYCLE DATA Cn[6:0]
PULSE WIDTH DATA Wn[3:0]
REFERENCE CLOCK

FIG.11

DIMMER ADJUSTMENT DATA

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	DIMMER VALUE (TW/T)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
					≀					≀
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	IMPOSSIBLE TO SET

(a)



(b)

FIG.12

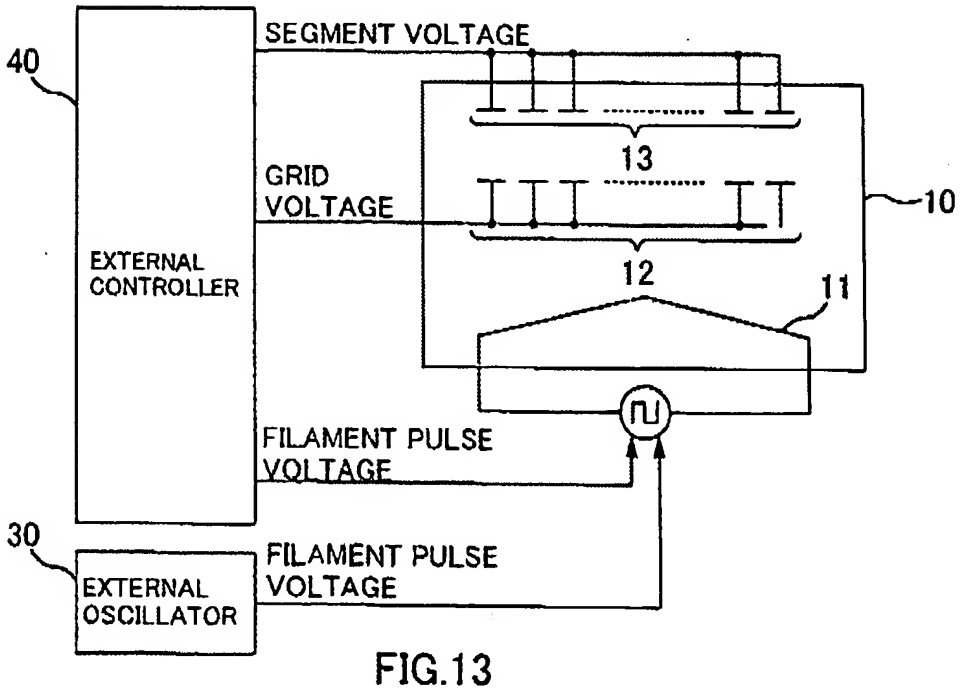


FIG.13

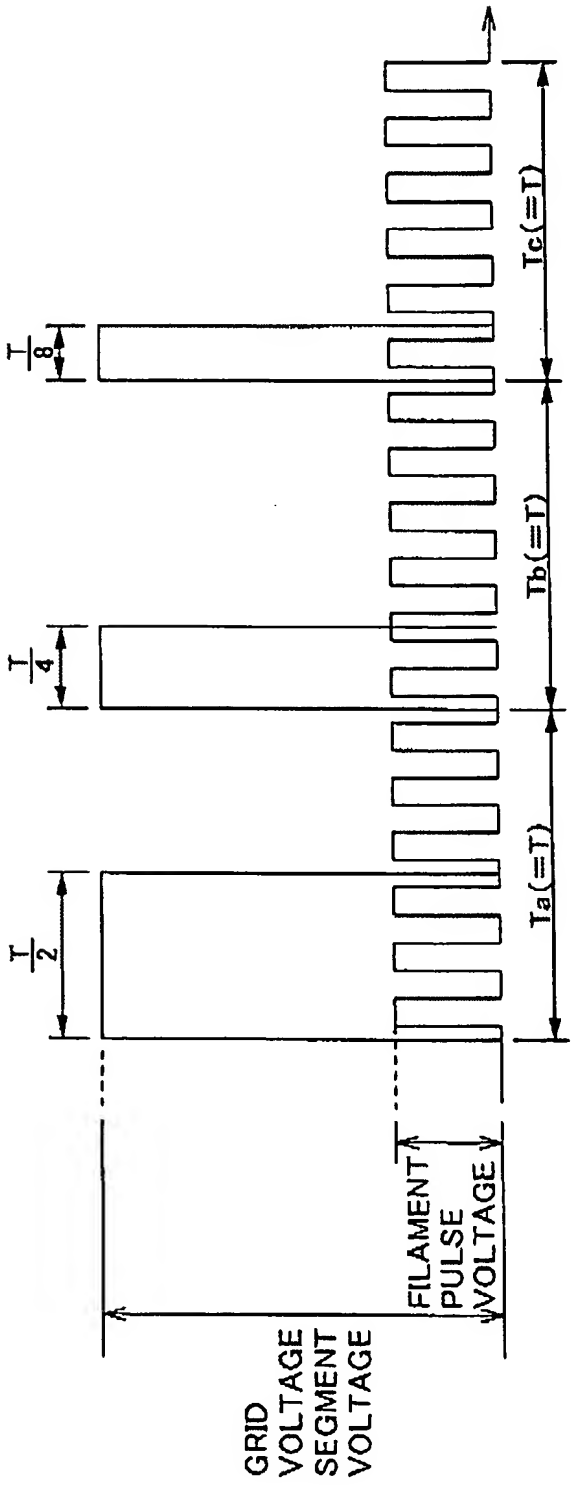

GRID VOLTAGE
SEGMENT VOLTAGE
FILAMENT PULSE VOLTAGE
T/2
T/4
T/8
Ta(=T)
Tb(=T)
Tc(=T)

FIG.14